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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/709,752	05/26/2004	Kohichi Ohsumi	JP920030018US1	3751

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INTERNATIONAL BUSINESS MACHINES CORPORATION
DEPT. 18G
BLDG. 321-482
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EXAMINER	
CHANG, RICK KILTAE	

ART UNIT	PAPER NUMBER
3726	

MAIL DATE	DELIVERY MODE
02/27/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/709,752	OHSUMI ET AL.	
	Examiner	Art Unit	
	Rick K. Chang	3726	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 December 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 12/23/08 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1 and 5-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Larson (US 5,160,579) in view of Hirose et al (US 6,591,495).

Re claims 1, 5: Larson discloses preparing an insulating substrate (10) having a front surface and a back surface, and a layer of metal foil (12) formed on at each one of said front surface and said back surface, said metal foil having an up surface (above 12 in Fig. 1A); selectively forming or forming an opening (a through hole in Fig. 1A) in a metal foil of one of said metal foils and said insulating substrate; forming a first resist pattern (16) on said metal foil; forming a plating layer (18) on an inner surface of said opening and areas of an up surface of said metal foil not covered by said first resist pattern; adjusting a thickness of said plating layer on said metal foil (col. 4, line 52), except for forming areas of said up surface of said metal foil

not covered by said plating layer into one or more lines, said one or more lines being separated from said area of said up surface covered by said plating layer and including a portion of said up surface.

Hirose disclose forming areas of said up surface of said metal foil not covered by said plating layer into one or more lines, said one or more lines being separated from said area of said up surface covered by said plating layer and including a portion of said up surface (88).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Larson by forming areas of said up surface of said metal foil not covered by said plating layer into one or more lines, said one or more lines being separated from said area of said up surface covered by said plating layer and including a portion of said up surface, as taught by Hirose, for the purpose of forming a multilayered printed circuit board.

Re claim 6: Larson discloses removing said first resist pattern (16 removed in Fig. 1I); forming a second resist pattern (20,22) on said areas of said metal foil; selectively forming an exposed portion of said areas of said metal foil using said second resist pattern (Fig. 1I); etching said metal foil at said exposed portion (12,14 removed); and removing said second resist pattern (20 removed).

4. Claims 3 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Larson (US 5,160,579)/Hirose et al (US 6,591,495) as applied to claims 1, 5-6 above, and further in view of Shipley (US 4,902,610).

Larson/Hirose fail to disclose forming a dielectric layer on said insulating substrate and on said plating layer and said lines on said metal foil; forming an opening in said plating layer; and performing plating on said opening.

Shipley discloses forming a dielectric layer (3) on a substrate (2) and on said lines (1); forming an opening (openings above 1 in Fig. 2) in said dielectric layer on the land; and performing plating on said opening (6).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Larson/Hirose by forming a dielectric layer on said insulating substrate and on said plating layer and said lines on said metal foil; forming an opening in said plating layer; and performing plating on said opening to the Larson/Hirose's PCB, as taught by Shipley, for the purpose of electrically communicating the inner circuits to the exterior circuits.

5. Claims 2 and 8-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Larson (US 5,160,579)/Hirose et al (US 6,591,495) as applied to claims 1, 5-6 above, and further in view of Tamm et al (US 5,666,722).

Larson/Hirose fail to disclose polishing a surface of said plating layer.

Tamm discloses polishing a surface of said plating layer (Fig. 2f).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Larson/Hirose by polishing a surface of said plating layer to the Larson/Hirose's PCB, as taught by Tamm, for the purpose of meeting the electrical requirements of the final circuit.

6. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Larson (US 5,160,579)/Hirose et al (US 6,591,495)/Tamm et al (US 5,666,722) as applied to claims 1-2 above, and further in view of Shipley (US 4,902,610).

Larson/Hirose/Tamm fail to disclose forming a dielectric layer on said insulating substrate and on said plating layer and said lines on said metal foil; forming an opening in said plating layer; and performing plating on said opening.

Shipley discloses forming a dielectric layer (3) on a substrate (2) and on said lines (1); forming an opening (openings above 1 in Fig. 2) in said dielectric layer on the land; and performing plating on said opening (6).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Larson/Hirose/Tamm by forming a dielectric layer on said insulating substrate and on said plating layer and said lines on said metal foil; forming an opening in said plating layer; and performing plating on said opening to the Larson/Hirose/Tamm's PCB, as taught by Shipley, for the purpose of electrically communicating the inner circuits to the exterior circuits.

7. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Larson (US 5,160,579)/Hirose et al (US 6,591,495)/Shipley (US 4,902,610) as applied to claims 5-7 above, and further in view of Tamm et al (US 5,666,722).

Larson/Hirose/Shipley fail to disclose polishing a surface of said plating layer.

Tamm discloses polishing a surface of said plating layer (Fig. 2f).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Larson/Hirose/Shipley by polishing a surface of said plating layer to the Larson/Hirose/Shipley's PCB, as taught by Tamm, for the purpose of meeting the electrical requirements of the final circuit.

8. Claims 11-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Larson (US 5,160,579)/Hirose et al (US 6,591,495)/Tamm et al (US 5,666,722) as applied to claims 5-6, 8-9 above, and further in view of Asai et al (US 6,828,510).

Larson/Hirose/Tamm fail to disclose polishing using a belt sander.

Asai discloses polishing using a belt sander (col. 23, line 49).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Larson/Hirose/Tamm by polishing using a belt sander to the Larson/Hirose/Tamm's PCB, as taught by Asai, for the purpose of meeting the electrical requirements of the final circuit.

9. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Larson (US 5,160,579)/Hirose et al (US 6,591,495)/Shipley (US 4,902,610)/Tamm et al (US 5,666,722) as applied to claims 5-7, 10 above, and further in view of Asai et al (US 6,828,510).

Larson/Hirose/Shipley/Tamm fail to disclose polishing using a belt sander.

Asai discloses polishing using a belt sander (col. 23, line 49).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Larson/Hirose/Shipley/Tamm by polishing using a belt sander to the Larson/Hirose/Shipley/Tamm's PCB, as taught by Asai, for the purpose of meeting the electrical requirements of the final circuit.

Response to Arguments

10. Applicant's arguments with respect to claims 1-13 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

11. Please provide reference numerals (either in parentheses next to the claimed limitation or in a table format with one column listing the claimed limitation and another column listing corresponding reference numerals in the remark section of the response to the Office Action) to all the claimed limitations as well as support in the disclosure for better clarity (optional). Applicants are duly reminded that a full and proper response to this Office Action that includes any amendment to the claims and specification of the application as originally filed requires that the applicant point out the support for any amendment made to the disclosure, including the claims. See 37 CFR 1.111 and MPEP 2163.06.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Rick K. Chang whose telephone number is (571) 272-4564. The examiner can normally be reached on 5:30 AM to 1:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David P. Bryant can be reached on (571) 272-4526. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Rick K. Chang/
Primary Examiner, A.U. 3726

RC
February 27, 2009